COEN 171 Design Project 2 Specifications

Due: Monday, April 6, 2009

1. Introduction and Objectives

The objective of this project is to begin the process of designing the building blocks that you will need in order to design the hardware system for an instruction set architecture in the final project. Specifically, you will design and simulate three datapath components:

- Register file
- Arithmetic Logic Unit
- Memory Unit

This project is to be implemented with *two-person teams*. You are allowed to discuss issues of a theoretical nature with other teams, however, you may NOT discuss specific design details.

2. Verification and Performance Evaluation.

There are two aspects of the evaluation process: verification and performance analysis. Verification involves testing and documenting that all designs work in accordance with the specification provided. Performance analysis involves measuring performance of your design with respect to a specific benchmark, in this case timing analyses that will be used to help you identify the maximum clock rate of your system. All verification and performance analysis procedures should be described in detail in your written report.

3. Design and Simulation Software

You will be using the Xilinx Integrated System Environment (ISE) for schematic design entry and simulation. The Xilinx software is installed in the COE 4th floor computer labs and EN 388. All design files and reports will be turned in electronically by zip file via D2L's digital drop box.

4. Project Report

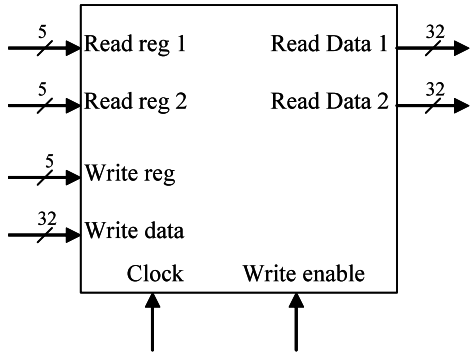
You will need to describe and justify your design choices in a written report. All aspects of your design should be presented. Grading will be based on how well you meet the goals of the project, on the performance of your hardware, and on the report itself. You should include at least the following sections.

1. Introduction/Summary of the project. This should include a short but complete executive summary that states clearly whether the components have been successfully tested, gives final performance numbers, and identifies bonus eligibility.
2. Discussion and justification of your design decisions and process
3. Full design specifications and schematics
4. Discussion of testing/verification approach and supporting simulations
5. Performance analysis of your components
6. Conclusions and discussion of what you learned.

5. Detailed Design Guidelines

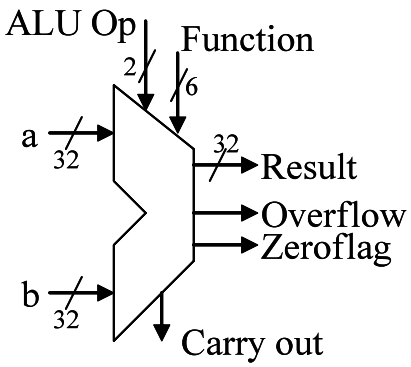
The three components you will be designing and simulating include:

Register File



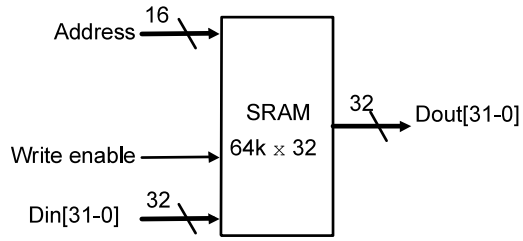
A register file, as discussed in class and the text, is simply a set of registers that can be read from and written to. You will implement a register file with 32 registers of 32 bits each. The register file should be designed using schematic entry in Xilinx; however, components inside the register file such as multiplexors may be created with Xilinx's Coregen tool if desired.

Arithmetic Logic Unit



The Arithmetic Logic Unit (ALU) is one of the most fundamental building blocks for computer hardware. You will implement a 32-bit ALU with capability to perform ADD, SUB, AND, OR, SLT, and SRL, along with zero-check and overflow indicators. (Note: SLT must work even in overflow situations.) The ALU may be designed using schematic entry in Xilinx or using HDL. Use any ALU design approach you wish.

Memory Unit



Capability to read and write information to memory is essential to all computer programs. You will implement a 64k x 32 (256kB) Static Random Access Memory (SRAM), i.e. a 16-bit wide address bus and a 32-bit wide data bus. The memory unit may be designed using any approach you wish, including hierarchical schematic design, HDL, or Coregen. The key design criteria is that the memory should be able to be *preloaded* with data using a hex text file (or other similar simple method).

6. ALU Instruction Bonus (0-5 points per each additional operation)

A bonus is available for designing additional functionality into the ALU unit (this may be valuable for the third project as well, to support a larger instruction set). Each new tested and verified ALU operation will receive 0-5 points, depending on the complexity of the circuits required (similar instructions requiring the same structure will receive bonus points as a group).

7. ALU Efficiency Bonus (maximum 10 points)

A bonus is available for designing a carry-lookahead (or similar fast adder design) ALU unit. The circuits for this must be designed in a hierarchical fashion using schematic entry or VHDL.