1. 1) For the MIPS code below, what is the corresponding C code?

```
Loop: sll $t1, $s3, 2
      add  $t1, $t1, $s6
      lw   $t0, 0($t1)
      bne  $t0, $s5, Exit
      addi $s3, $s3, 1
      j    Loop
Exit:
```

2. What are the two fallacies and single pitfall of pipelining?
   Pipelining is easy. Pipelining ideas can be implemented independent of technology. Failure to consider instruction set design can adversely impact pipelining.
3. For the code sequence below, indicate whether it must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding:

```
addi $t1, $t0, 1
addi $t2, $t0, 2
addi $t3, $t0, 2
addi $t3, $t0, 4
addi $t5, $t0, 5
```

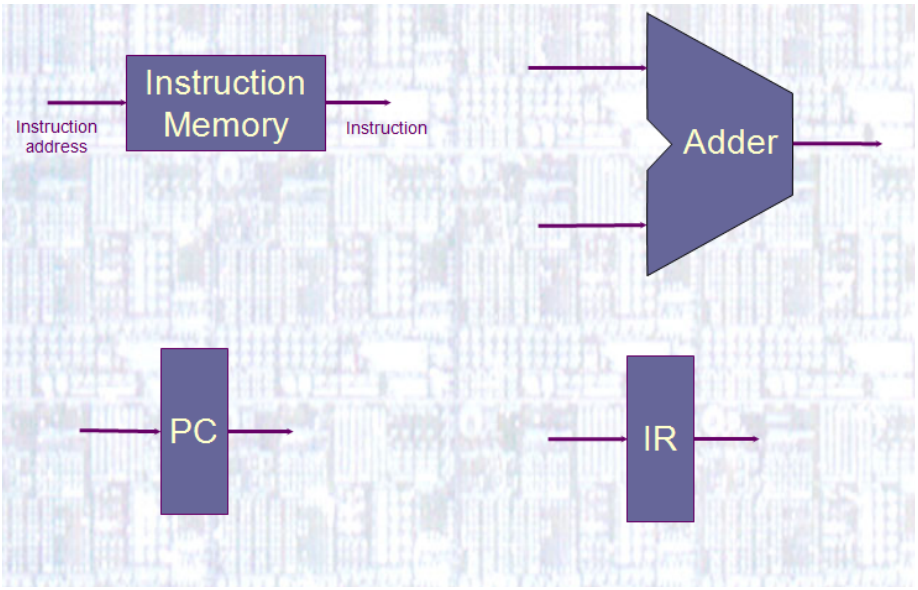
4. The following MIPS code can cause what type of hazard?

```
add $s0, $t0, $t1
sub $t2, $s0, $t3
```

5. A new processor can use either a write-through or write-back cache selectable through software. Assume the processor will run data intensive applications with a large number of load and store operations. Which cache write policy should be used?
6. List the 4 principles of hardware design.
   - Simplicity favors regularity
   - Smaller is faster
   - Make the common case fast
   - Good design demands compromise
7. Explain what is meant by overflow and underflow.
   - Overflow occurs when an operation results in a number that is too big to be represented in the available storage space.
   - Underflow occurs when an operation results in a number that is too small to be represented in the available storage space. It is basically a negative overflow.
8. What are the 5 stages of the MIPS pipeline?
   - IF: Instruction fetch from memory

- ID: Instruction decode and register read
- EX: Execute operation or calculate address
- MEM: Access memory operand
- WB: Write result back to register

9. Explain temporal and spatial locality.
   Temporal locality: if an item is referenced, it will tend to be referenced again soon.
   Spatial locality: if an item is referenced, items whose addresses are close by will tend to be referenced soon.
10. Connect the hardware to implement the fetch and execute cycle.



11. The “factory” analogy of a computer has 6 parts to it. Name the each of the 6 parts of this analogy and give two examples of each.
12. In binary arithmetic, there are four situations from which an overflow can arise. List all four situations. List three possible ways to handle an overflow.
13. There are two common categories of ISAs. Name and describe them both and list some advantages and disadvantages of both
14. There are five stage of the MIPS pipeline. List the stages, and state which step is taken at every stage.
15. List the three types of hazards talked about in class and give a brief description of each one.
16. What are spatial and temporal locality and how are these taken advantage of in a processor?
17. How are miss rates and the level of memory association related and what kinds of trade-off need to be made?
18. What extra hardware is needed for a pipelined architecture?

19. What factors impact the complexity of a pipelined architecture?
20. Which processor is faster? P1 has a CPI of 1.5 and a clock rate of 2 GHz. P3 has a CPI of 2.5 and a clock rate of 3 GHz.
21. List the five stages of a pipelined datapath and define them.
22. Define the Least Recently Used (LRU) replacement scheme for caches and explain why it is most commonly used.
23. Explain why hazards exist when pipelining is used and how they can be avoided.
24. When should dynamic branch prediction be used over a static prediction scheme?
25. Define the following terms: latency, throughput, and execution time.
26. Name and describe the two different types of locality.
27. In a certain CPU implementation, the number of clock cycles to execute several types of instructions is shown below.

Instruction Type	# of cycles
Load	10
Store	8
R-Type	4
Branch	6
Jump	5

- A program's instructions are distributed as shown below; calculate the average CPI of the processor

Instruction Type	% of instructions
Load	15%
Store	25%
R-Type	50%
Branch	8%
Jump	2%

- If the clock speed is 2MHz, how long will it take a program of 1,000,000 instructions to execute?
- If the CPI of store instructions can be cut in half, what will be the new average CPI?

28. Explain why an n-stage pipeline will not create an n-fold performance increase.
29. Consider the following two binary numbers

```
A:   01011101
B:   10010010
```

- Find A+B and check for overflow; assuming A and B are unsigned integers.

- Find A-B and check for overflow; assuming A and B are integers represented in 2's complement

30. Explain the structure of a memory hierarchy
31. Describe the three main types of hazards (structural, data, and control) and give one possible solution for each. Assume the MIPS instruction set is used.
32. What is branch prediction? Describe the two main types of branch prediction.
33. Identify the hazard(s) in the following MIPS code segment:

```
loop:  add  $t0, $t1, $s1
       add  $t2, $t0, $s2
       beq  $t2, $s0, loop
       sw   $t0, 0($s3)
```

34. Regarding memory, what is the difference between spatial locality and temporal locality?
35. True or False: Pipelining is technology-independent. Explain.

36. Assume that the following instruction is read from instruction memory:

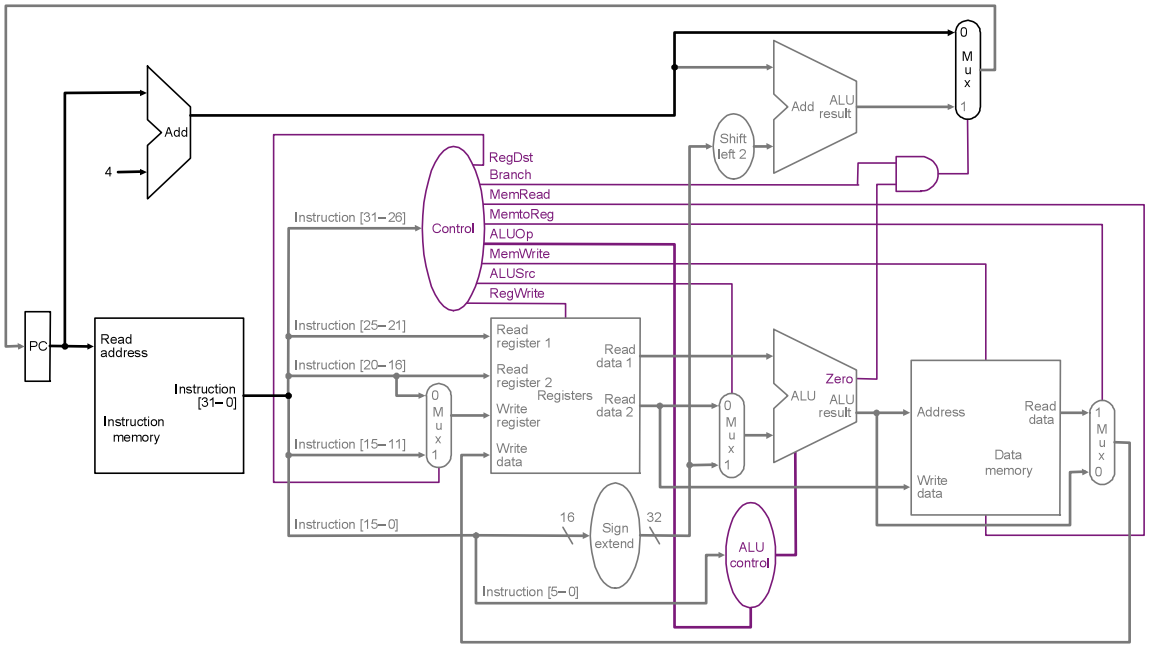
add $s0, $a1, $t7

The binary equivalent of this *add* instruction is shown below:
Instruction[31-0]:

op	rs	rt	rd	shamt	funct
000000	00101	01111	10000	00000	100000

Provide the binary values of the following input and control lines from single cycle data path diagram shown below.

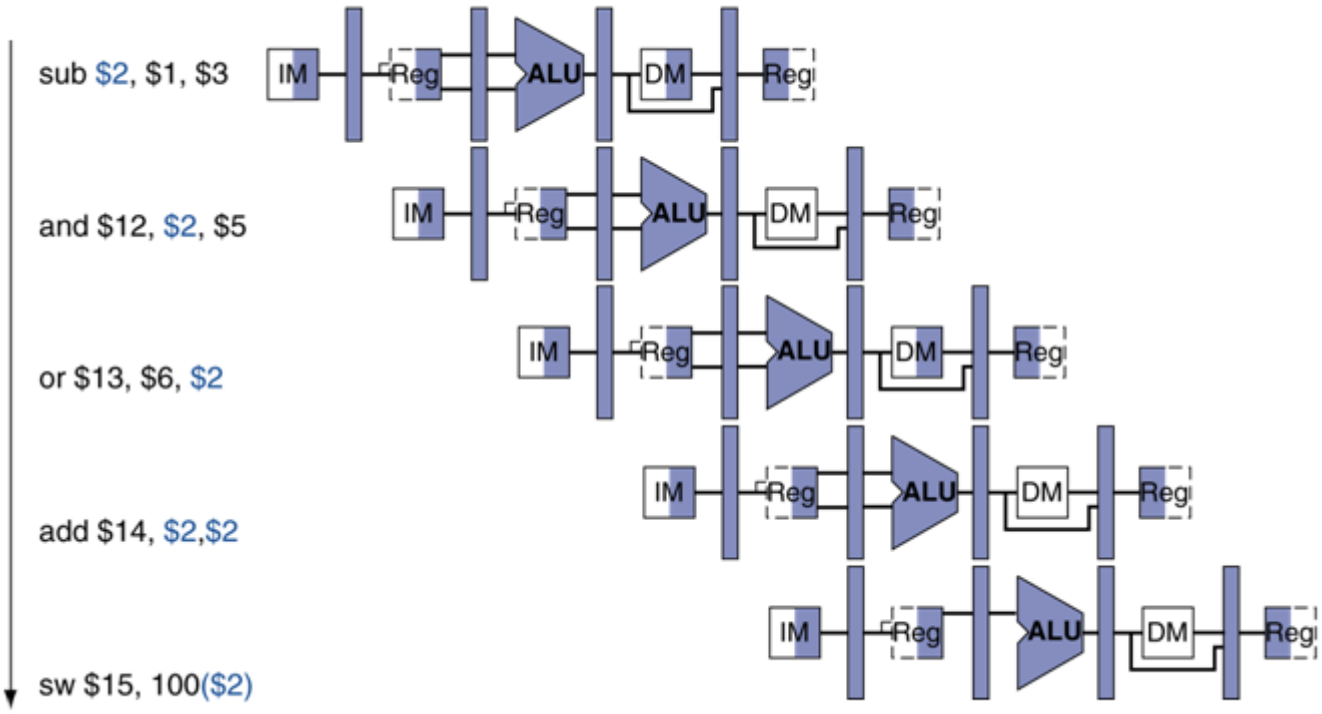
- Instruction[31-26]:
- Read register 1:
- Read register 2:
- Write register:
- RegDst:
- ALUSrc:
- MemtoReg:
- RegWrite:
- MemRead:
- MemWrite:
- Branch:
- Jump:
- AluOp[1-0]:



37. Pipelining is a common technique used in current processor architectures. Explain why a pipelined implementation is used in place of a single cycle CPU mplementation (Hint: how would the clock speed be determined in a single cycle CPU implementation)? What are some of the difficulties associated with implementing a pipelined architecture?

38. From the set of instructions below, show what data needs to be forwarded by drawing any necessary connections on the pipeline diagram that follows.

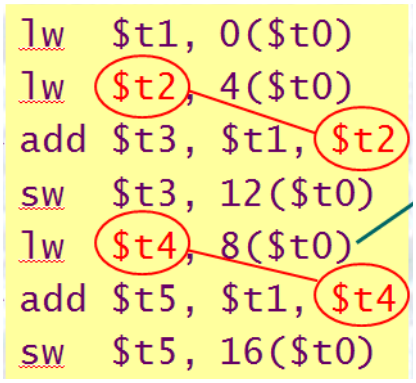
```
sub  $2,  $1,  $3
and   $12,     $2,  $5
or   $13,      $6,  $2
add  $14,      $2,  $2
sw   $15,      100($2)
```



39. Consider a cache with 64 blocks, where each block is composed of 16 bytes. If we assume that this cache is using direct mapping, what block does the memory at byte address 528 get mapped to?
40. What are the four design principles on which the MIPS ISA is based?
41. List the four principals of hardware design.
42. In response to the Power Wall, CPU clock rates have not risen but fallen, yet computer performance has not, explain this phenomenon?
43. True or false, designing a pipelined processor is easy? Explain why or why not.
44. System cache can either be implemented using direct map or associative, ideally one would like to use a fully associative implementation, why is this not possible?
45. Fill in the blank:
    - The valid bit implies a bit is ¬_____. (Do not use the word valid)
    - The dirty bit implies a location has been _____.
46. What are data path and control?
47. Connect the following circuit to form the R-Format data path and control.

48. What are some specification advantages to micro-coding and implementation advantages and disadvantages?
49. What is the difference between a structure hazard, data hazard and control hazard?

50. Below is a snippet of code. Determine where there might be stalls in a pipeline architecture and rearrange the line of coding to remove the stalls in the coding.



51. What is pipelining? What are some possible hazards of pipelining, and what are some solutions for the hazard?
52. How do modern computers get past the power wall problem? Why does it work? Are there any drawbacks to the solution?
53. What are the 5 stages of the datapath does the MIPS processor take advantage of for pipelining?
54. What is the memory heirarchy? Why is it needed? What are the general characterstics of memory as you go from high levels to levels in the heirarchy?
55. How does an access in direct mapped cache work? What happens if the requested data is not in the cache?
56. What is the disadvantage of having a single-cycle architecture?
57. What are the 5 steps of a MIPS instruction?
58. Define structural hazard:
59. The concept of pipelining improves performance by increasing _____ _____, as opposed to decreasing _____ _____ of an individual instruction.
60. When dealing with data hazards, extra hardware is added to retrieve missing data early from the internal resources is called:
61. What are the four underlying principles of hardware design (briefly explain)?
62. Write the equation for calculating computer performance (CPU time in seconds). Name several components that affect CPU time performance:
63. Draw the complete datapath for an R-type instruction. Write the four main components of this instruction cycle.
64. What are the 5 stages of MIPS pipelining
65. Name the three hazards category for pipelining. Give possible solutions for each hazard.

66. Convert the decimal number 28 into sign and magnitude, 1's complement, 2's complement, octal, and hexidemical. Convert the decimal number -5 into. Sign/magnitude, 1's complement, and 2's complement. What are the advantages of 2's complement? What is an advantage of hexadecimal numbers with respect to binary?
67. What are the parts of the instruction cycle?
68. Which computer can execute each instruction faster? Computer A: Cycle Time = 250ps, CPI = 2.0 and Computer B: Cycle Time = 500ps, CPI = 1.2.
69. What are some advantages to a smaller PLA?
70. What are some microcode advantages and disadvantages?
71. Explain pipelining using laundry and the following image and elucidate the speed increase for doing laundry. Then give some advantages and disadvantages of pipelining.
72. Provide an example of a data hazard, and briefly show where the hazard lies. Provide a workaround for the data hazard. Provide an example of a control hazard, and briefly show where the hazard lies.
73. What is the relationship between capacity and speed that is typical in all kinds of computer memory? Why is this the case?
74. List 2 differences between the R-type instruction data path, and the I-type instruction data path. List 2 differences between the I-type instruction data path, and the J-type instruction data path. List two responsibilities of the processor control unit in a datapath.
75. Determine if the following instruction is an R-type, I-type, or J-type instruction, and then decode it. 0000 0001 0000 0000 0000 2000 0010 0000
76. Which instruction type allows shifting? By how much can a number be shifted? Why? What is the range of jump addresses? Why? What is the largest number the MIPS architecture can compare in Immediate-type instructions?
77. Give the abbreviations and descriptions for the five stages of the MIPS Pipeline?
78. Give the name and a brief description of the three types of pipelining hazards?
79. What are three methods for avoiding data hazards?
80. What are the four basic principles of computer design?
81. What are the benefits and drawbacks of fully associative cache vs. direct mapped cache?

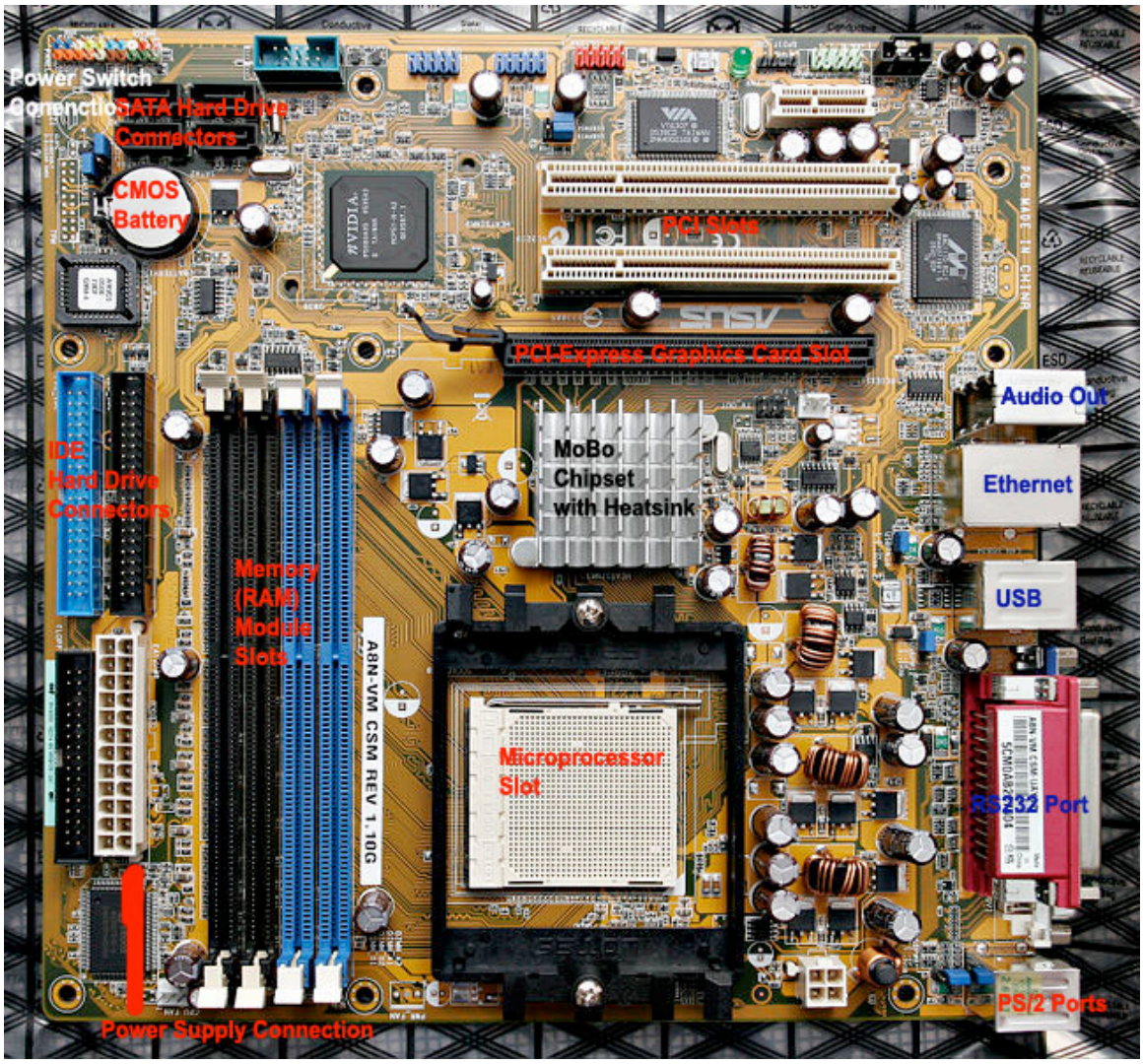
82. What does the following Verilog code accomplish?

```
module testquestion(
    input [31:0] Din,
    input [15:0] Address,
    input WriteEnable,
    input clock,
    output reg [31:0] Dout
    );

   parameter RAM_WIDTH = 32;//A 32 bit wide data bus
   parameter RAM_ADDR_BITS = 16;//A 16 bit wide address bus

   /*Set the size of SRAM to 64k x 32*/
   reg [RAM_WIDTH-1:0] SRAM [(2**RAM_ADDR_BITS)-1:0];

   /*Read in data preloaded from a hex text file*/
   initial
      $readmemh("memtest.txt", SRAM);
   /*Set SRAM at the Address to Din if clock and write enable are
1*/
   /*Then set Dout to be that value of SRAM at address*/
   always @(posedge clock) begin
      if (WriteEnable)
         SRAM[Address] <= Din;
      Dout <= SRAM[Address];
   end

endmodule
```

83. What does the following Verilog code accomplish?

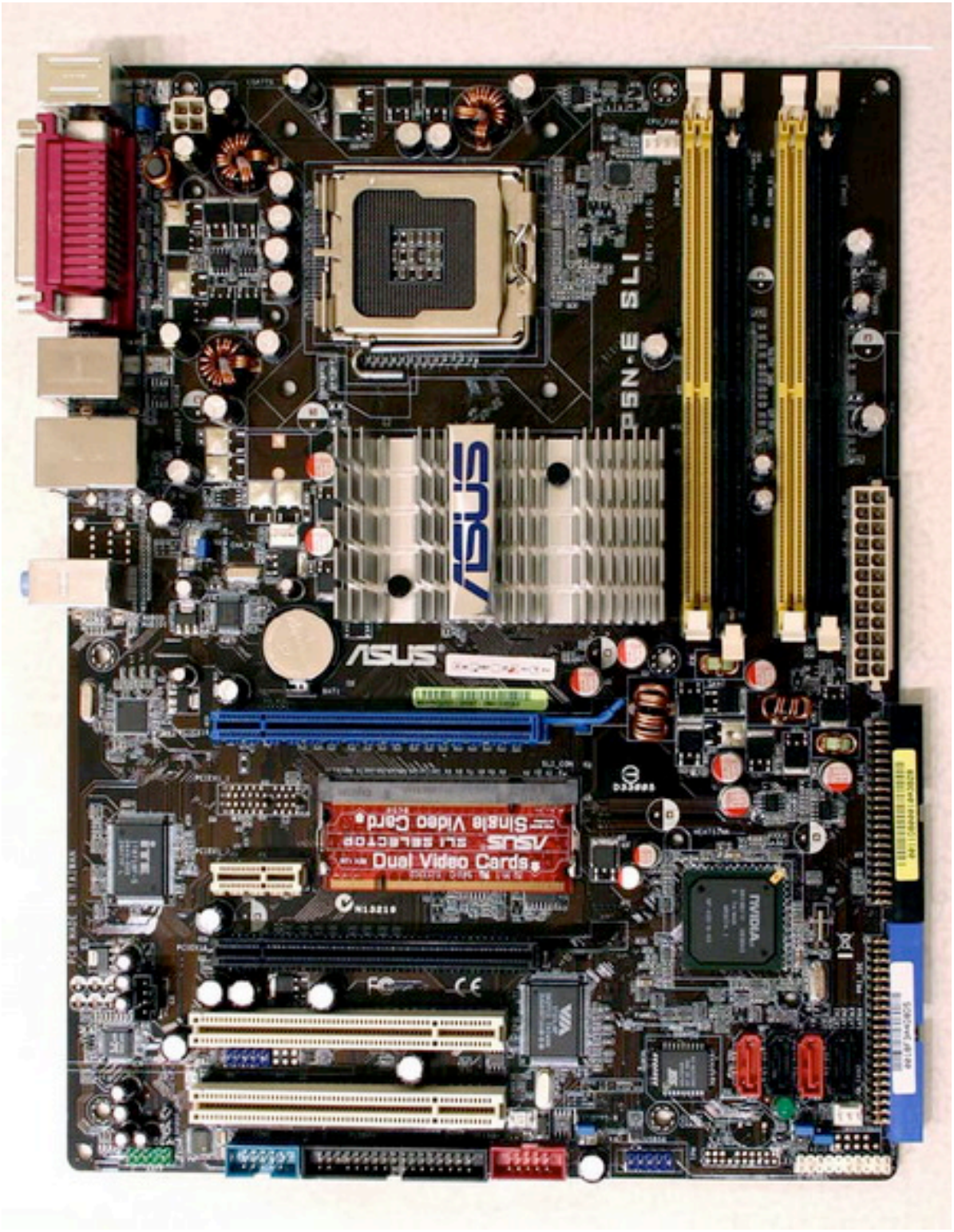
```
module testquestion (ALUOp, Function, A, B, ALUOut, Overflow, Zeroflag, COut);
	input [1:0] ALUOp;//The ALU Op Code
	input [5:0] Function;//The Funct
	input [31:0] A,B;//Inputs

	output reg [31:0] ALUOut;//The output after performed operation
	output Overflow;//Overflow bit
	output Zeroflag;//The zeroflag
	output COut;//The carryout

	assign Zeroflag = (ALUOut==0); //Zeroflag is true if ALUOut is 0

	always @ (ALUOp or Function or A or B)
	begin
	if (ALUOp == 2 && Function == 36)
		ALUOut <= A & B;//and
	else
	if (ALUOp == 2 && Function == 37)
		ALUOut <= A | B;//or
	else
	if (ALUOp == 2 && Function == 32)
		ALUOut <= A + B;//add
	else
	if (ALUOp == 2 && Function == 34)
		ALUOut <= A - B;//sub
	else
	if (ALUOp == 2 && Function == 42)
		ALUOut <= A < B ? 1:0;//slt
	else
	if (ALUOp == 2 && Function == 0)
		ALUOut <= A << B;//shift left
	else
	if (ALUOp == 2 && Function == 2)
		ALUOut <= A >> B;//shift right
	else
	if (ALUOp == 2 && Function == 39)
		ALUOut <= ~(A | B);//nor
	else
	if (ALUOp == 2 && Function == 38)
		ALUOut <= A^B;//xor
	else
	if (ALUOp == 2 && Function == 40)
		ALUOut <= A~^B;//xnor
	else
		ALUOut <= 0;//If the opcode is not 2, then output 0
	end
endmodule
```

84. Label the following motherboard parts:



85. Express 14, -14, 25, and -25 in One's Complement, Two's Complement, and Sign and Magnitude.
86. List the 4 Principles of hardware design.
87. Define sign overflow and specify how we can check to see if it has occurred.
88. What are the four design principles discussed in chapter 2?
89. List the three different types of memory technologies from fastest to slowest and describe them.
90. List advantages and disadvantages of pipelining.
91. What are the four types of addressing in MIPS?

92. Label the components on the motherboard image below:



93. What are the four Instruction Set Architecture (ISA) design principles?
94. Represent 15, -15, 20, -20, 31, and -31 in six-bit two's complement binary notation.
95. Complete the ALU unit written in Verilog. Assume these control values for the operations:
    - 0: Bitwise AND;
    - 1: Bitwise OR;
    - 2: Addition;
    - 6: Subtraction;
    - 7: SLT;
    - 12: Bitwise NOR.
    - Also be able to handle other control input values.

    module MIPSALU (ALUctl, A, B, ALUOut, Zero);

96. Is it easier to implement pipelining for a RISC architecture or a CISC architecture? In either case, what should you watch out for while implementing pipelining?
97. What are the two types of caching called? What are the two types of localities that are used to make cache memory perform faster?
98. What are the three pieces of information that must be stored in cache for each word?
99. When a hazard occurs, a bubble/stall can be inserted in the pipeline, but this slows down the pipeline and degrades processor performance. There are two alternatives that avoid stalling – what are they?
100. What are the five stages of the MIPS pipeline?
101. What are the main pro and con (1 of each) of increasing associativity in an associative cache?
102. Define both spatial locality and temporal locality.
103. Explain the difference between Direct Map and Associative cache structures.
104. Describe Hit time, hit rate, miss rate, and mess penalty.
105. Identify the Five Stages of Load.
106. How many total bits are required for a direct mapped cache with 16KB of data and 4-word blocks with 32-bit address?
107. Name all three Pipeline Hazards and define them
108. What are the Five Stages of a Datapath?
109. What are the two types of Locality?
110. Add 45 and -38 in 2's complement format. Use 8-bits.
111. Name two types of Branch Prediction and define them.

112. What three things comprise of the most basic computer:
113. All computers are made up of these things, and build upon these things. Give one example of how these three things are made into a more complicated system.
114. In the pipelining process, what is a hazard?
115. What are the names of the three kinds of hazards discussed?
116. Why do each of the above hazards cause problems?
117. Assuming that the following code is placed in a pipeline, what potential problem lies within the code? Give an example of how this problem can be fixed on a hardware level.

```
sub     $2, $1,$3
and     $12,$2,$5
or      $13,$6,$2
add     $14,$2,$2
sw      $15,100($2)
```

118. Give an analogy that explains why the concept of pipelining is easy at its basic idea.
119. What complicates things in the pipeline? Give an example of one.
120. The Principle of Locality plays a vital role in the way that data is stored in the computer memory. Explain what the Principle of Locality is, then explain the difference between temporal locality and spatial locality. In doing so, make sure to give practical programming usages of each type.
121. If the clock rate is 5GHz and the IPC = .4, what is the MIPS rating?
122. If A =0E26 and B =B4CA what is their sum if they represent 16 bit unsigned hexadecimal numbers? The result should be in Hexadecimal.
123. What are A and B in decimal assuming they are a) unsigned? b)sign and magnitude?
124. A computer is basically:
    - a bunch of multiplexors and gates to be an ALU
    - an interface memory
    - controlled by a bunch of gates to tell the first bunch of gates what to do, sequenced by an all-controlling clock edge
    - all of the above
125. R-type Instruction stands for _____ Format?
126. I-type Instruction stands for _____Format?
127. J-type Instruction stands for _____Format?
128. In MIPS code, OP and FUNCT are each ____ bits?
129. In MIPS , rs, rt, and rd are each_____bits?