1. A program's execution time is 100 seconds. Suppose FP instructions account for 30% of the execution time of the program and multiply instructions account for 10% of the execution time. How much faster would the program execute if we sped up FP instructions by a factor of 3 and multiply instructions by a factor of 5?

2. For the C code below, what is the corresponding MIPS code?

```
for(i=0; i != x; i++) {
      D[i] = D[i];
}
```

Assume that `$a0 = D[]` and `$a1 = x`

3. Translating MIPS Assembly Language into Machine Language

Translate the following instructions to MIPS machine language code:

a) `lw  $s1, 100($s2)`

op	rs	rt	rd	shamt	funct

b) `beq $s1, $s2, 25`

op	rs	rt	rd	shamt	funct

c) `addi $s1, $s2, 55`

op	rs	rt	rd	shamt	funct

d) `jr $ra`

op	rs	rt	rd	shamt	funct

4. Given the following bit patterns:

1) 0101 1001

2) 1010 0100

what does each pattern represent, if it is either of the following?

a.) an unsigned integer?
b.) a signed integer?
c.) Perform the following calculation using 2's complement:
$$-1) + 2)$$

5. Suppose the carry look ahead expression for the final 4-bit adder block of a 32-bit adder is:

$$c32 = G3 + P3G3 + P3P2G1 + P3P2P1G0 + P3P2P1P0c0$$

How many gates delays exist for the 32-bit carry look ahead adder?

6. List the 4 principles of hardware design.
7. Write the number -25 in sign and magnitude, 1's complement, and 2's complement.
8. Explain what is meant by overflow and underflow.
9. Control is the sequential logic that reconfigures the _____ to allow the _____ to flow properly through the hardware components.
10. Multiple Choice: In the MIPS architecture, the return address is stored in register number:

   a) 0

   b) 1

   c) 31

   d) 32

11. Recently, computer engineers have discovered a "speed wall" in the frequency clocking of CPUs. What method have computer engineers used keep increasing processing speed. Why does this not translate to a "perfect" increase in performance?
12. Explain the difference between Big Endian and Little Endian addressing modes.
13. Explain how to represent negative numbers using both 1s compliment and 2s compliment. Give an 4 bit example of each.
14. List at least three factors which influence how fast a process runs on a computer, and explain why the influence this speed.
15. Give three out of the 4 design principles of the MIPS architecture
16. Subtract the 8 bit, base 10 number 74 from the 8 bit, base ten number 109 using 2's compliment and show the result in hexadecimal format.
17. How many seconds does it take for each processor to complete running through its process

processor	speed	FP Inst	Int Inst.	L/S Inst.	Branch Inst.	CPI FP	CPI Int	CPI L/S	CPI Branch
P1	3GHz	230 million	750 million	2.1 billion	130 million	2	1	4	2
P2	2.4GHz	230 million	400 million	1.4 billion	130 million	1	1	4	6

18. Assuming $a0 = 10 and $a1 = 4, What is in the $v0 register when the following code completes?

add $t0 , $a0, $a1
sub $t1, $a0, $a1
sub $v0, $t0, $t1

19. Fill in the missing words from the following lines:

a. Simplicity favors _____ .
b. Smaller is _____.
c. Make the _____ case faster.
d. Good design demands _____.

20. There are three formats of MIPS instructions. Of what type are the following three instructions.

a. addu

0	rs	rt	rd	0	0x20

b. addi

8	rs	rt	n

c. beq

| 4	rs	rt	offset

21. Given a program with 100 instructions divided into classes as follows: 20% class A, 20% Class B, 20% Class C, and 40% class D, how fast is this implementation?

Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
1.7 GHz	2	2	1	3

22. Assume 1 GHz clock rate. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

# Processors	FP Inst	INT Inst	L/S Inst	Branch Inst	CPI (FP)	CPI (INT)	CPI (L/S)	CPI (Branch)
1	500×10^6	2130×10^6	1240×10^6	126×10^6	2	2	4	4

23. Label the following motherboard parts:
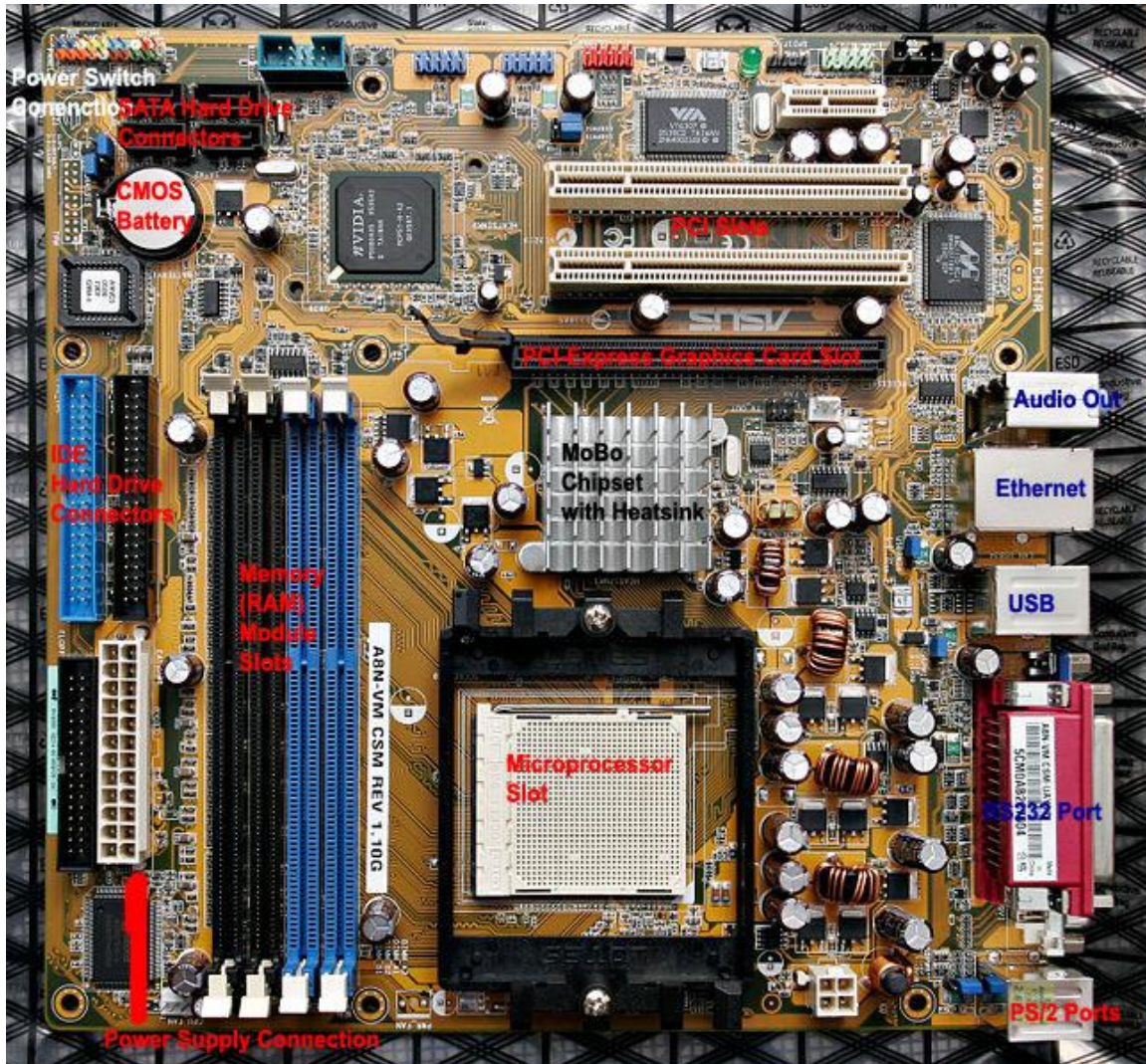
24. Multi Part Question: Express 14, -14, 25, and -15 in One's Complement, Two's Complement, and Sign and Magnitude.

25. Which of the following will affect performance?

    A. Algorithm
    B. Programming Language
    C. Compiler
    D. Instruction Set Architecture
    E. All of the above

26. Question: Define sign overflow and specify how we can check to see if it has occurred.

27. Question: Convert the following decimal number to 16bit signed hexadecimal and binary: 15,000

28. Question: What are the four design principles discussed in chapter 2?

29. Question: What are the four types of addressing in MIPS?

30. Question: How long is the OP code for a MIPS instruction?
    - A)   4 bits
    - B)   5 bits
    - C)   6 bits
    - D)   7 bits
    - E)   8 bits

31. Label the components on the motherboard image below:
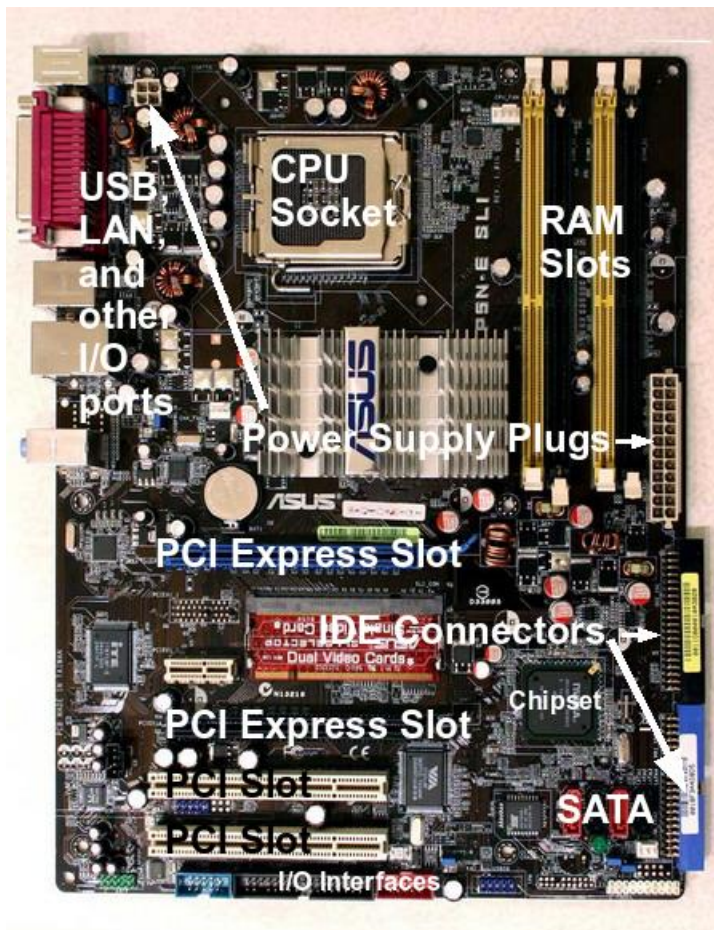
32. A and B are 16-bit numbers represented in hexadecimal. A = A1D2 and B = 062C. Perform the following operations and write the result in hexadecimal.

    a. A+B if A and B are unsigned.
    b. A+B if A and B are in sign-magnitude format.
    c. A-B if A and B are unsigned.
    d. A-B if A and B are in sign-magnitude format.
    e. A+B if A and B are in one's compliment.

f. A-B if A and B are in two's compliment.

33. Derive the logic equation for Zout and Zcarry to implement the ADD operation on a 1-bit adder using inputs A, B, and C (carry input).

34. Fill in the table for the following 1-bit ALU inputs. Assume operations 00 to 11 are available.

	A$_{Invert}$	B$_{Invert}$	CarryIn	Operation #
AND				
OR				
ADD				
SUB				
NOR				
SLT				

35. Evaluate the expressions by filling in the inputs and outputs for a 1-bit ALU. Assume numbers in parentheses to mean the carry bit, if applicable.

Exp	A	B	A$_{Invert}$	B$_{Invert}$	CarryIn	Op #	Output	CarryOut
1 & 0								
1 | 1								
1+0								
1+1								
1+1+(1)								
1-1								
1 NOR 1								

36. Given the following performance data...

Processor	Clock Rate	CPI
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

      a. Which processor has the highest performance?
      b. How many cycles and instructions for each processor if CPU time is 10 s?
      c. What should the clock rate be if we reduce the time by 30% and increase the
CPI by 20%?

37. For each of the problems below, assume the numbers are stored in 8-bit two's complement.

    1. Convert the numbers to their binary representations.
    2. Do the addition or subtraction in binary.
    3. Convert the result back to decimal (remember, it's 8-bit two's complement).
    4. State whether or not overflow occurs.

a) 45 + 87
b) 120 − 26
c) (-18) + (-99)
d) (-100) − 55

38. The four principles of designing computers are:

Simplicity favors _____.
Smaller is _____.
Make the _____ fast.
Good design demands _____.

39. Name the three instruction formats for MIPS.

40. A CPU has a clock rate of 2GHz and CPI of 1.2. If it takes a program 5 seconds to execute on this processor,

a) How many clock cycles did it take to execute the program?
b) How many instructions were executed?
c) You want to execute the same program in 3 seconds, so you increase the clock rate, but in doing so, the CPI increases to 1.5. How fast must the clock rate be to achieve the 3 second execution time?

41. In the diagram below, connect the components to indicate the datapath for an R-format instruction.
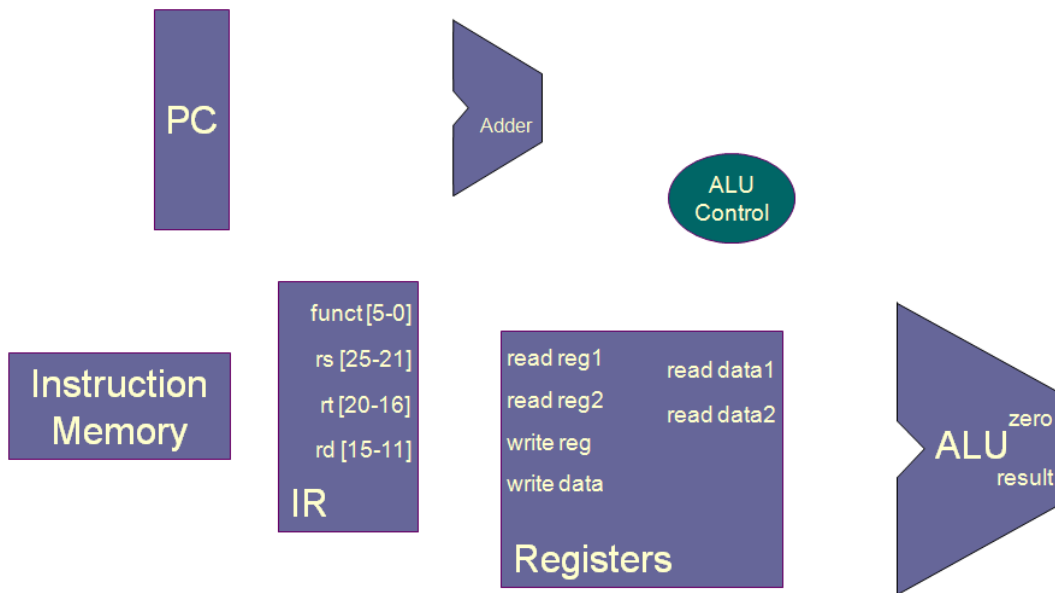

42. Describe each of the following types of MIPS addressing modes and provide instances in which each type would be used:

Immediate Addressing
Register Addressing
Base or Displacement Addressing

43. Suppose computer A runs the program in 20 seconds. Computer B is to be designed using to run the same program in 12 seconds. Computer A has a 3 GHz processor. Computer B will require 1.3 times as many clock cycles as computer A to complete the program. What clock rate should computer B have?

44. Using the table provided answer the following question. Assume the program being run uses 20 type A instructions, 10 type B, 5 type C, 40 type D and 8 type E. Calculate the total number of cycles to run the program, the CPI, and determine how long it would take this program to execute on a 2 GHz machine.

CPI for each instruction class				
A	B	C	D	E
1	2	3	1	3

45. List and explain the four Instruction Set Architecture Design Principles.

46. Add the following sets of numbers in 2's complement and indicate when an overflow has occurred. Use 4 bits.

    A. 2+5

    B. 5+7

    C. 4-7

    D. -4+7

47. Explain why growth in processor speeds has been slowing down as of late.

48. Also explain how designers of today's computers have worked around the problem given in (a).

49. What new problems arise with the workarounds described in (b)?

50. MIPS assumes there is a certain amount of bookkeeping that is done by the programmer. What does is assume the programmer will do at the beginning of each subroutine? at the end of each subroutine? Extra Credit: write the MIPS code outlined in your answer. (6 lines minimum)

51. Label as many parts as you can on the picture below:
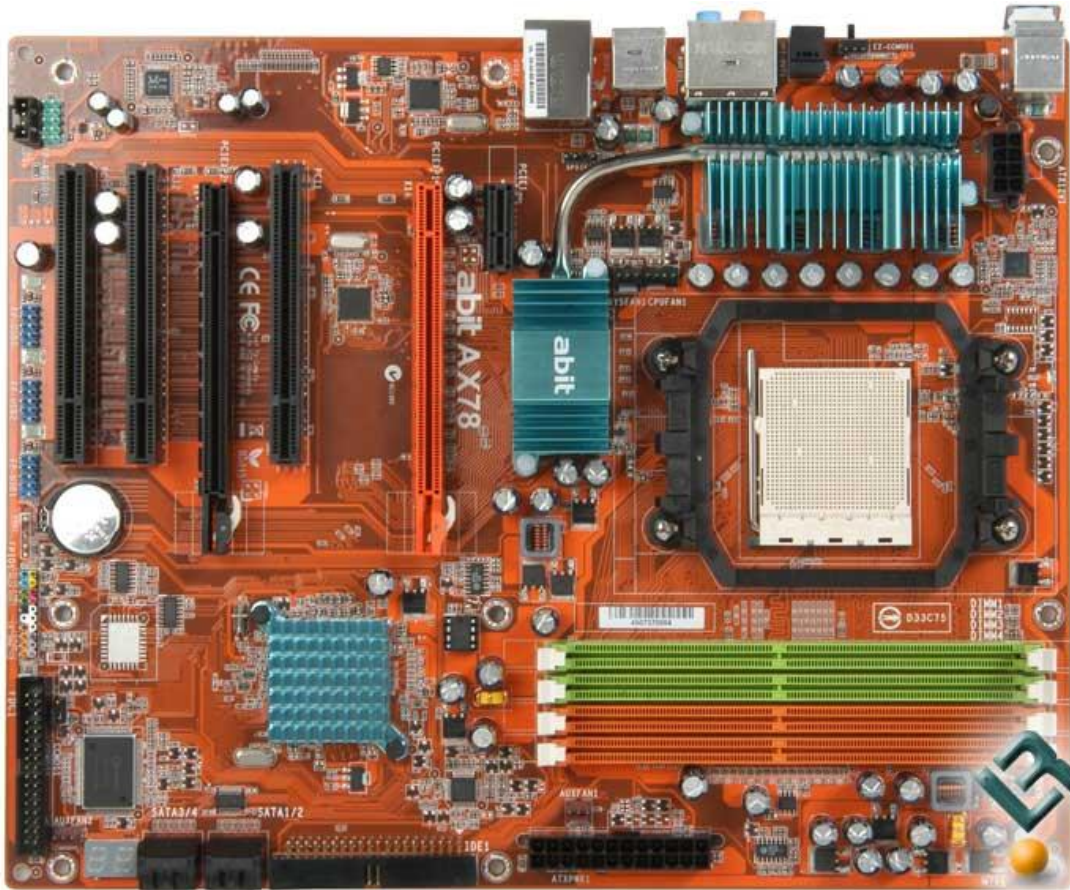
52. One issue that must be tackled when working with circuitry that does arithmetic is overflow. What are two cases where overflow is guaranteed to not occur?

53. What are three of the four ways that overflow can happen?

54. Match the following terms

___ 1. Throughput   a. Cycles per Instruction
___ 2. Performance   b. CPU Clock Cycles / Clock Rate
___ 3. Clock Cycles   c. Total work done per unit time
___ 4. CPI   d. Instruction Count x CPI
___ 5. CPU Time   e. Clock Cycles / CPU Time
___ 6. Clock Rate   f. 1 / Execution Time

55. Add 45 and -38 in 2's complement format. Use 8-bits.

56. What is the hardware that performs addition, subtraction, and logical operations such as AND and OR?
- Program Counter
- ALU
- Register
- CPU

57. The least significant bit refers to the rightmost bit in a MIPS word.   True or False
58. Almost all computers are constructed using a _____ that determines when events take place in the hardware.
    - CPU
    - ALU
    - Clock
    - PC

59. Improving one aspect of a computer will increase the overall performance of the computer. True or False
60. A program is written to perform vector addition. One of the high-level language instructions in the program is
    z= y + x[8]; Assume the base address of the int array x is stored in register $s0. Translate this instruction into an assembly language instruction.
61. If the CPI value for an R-format instruction is 1, the CPI for an I-format instruction is 5, and the CPI for a J-format instruction is 3, calculate the average CPI for this high-level language instruction.
62. If the clock rate for the machine this program is run on is 250MHz, calculate the time taken to run this high-level instruction.
63. Suppose the CPI for I-format instructions are successfully reduced to 4. Calculate the time taken to run the high-level instruction now.
64. Suppose we want the program to run two times as fast on the same machine, by reducing the average CPI of I- and J-format instructions. What must the average CPI of I- and J-format instructions be reduced to?

The MIPS architecture provides 32 general purpose registers.
65. How many registers are conventionally used to pass arguments? What happens when the number of arguments passed exceeds this number?
66. Why are 'callee-saved' registers referred to as callee-saved?
67. If a save of these callee-saved registers is necessary, where are they saved to? In what order are they saved? Does it matter?
68. Name two registers that programmers do not usually write over, and explain why they aren't used / written over.
69. Convert this pseudo-instruction into a 'real' assembly language instruction: move $t1, $t0.
70. Represent -26 and -17 in sign-and-magnitude notation.
71. Find the value of 35 - 26 and 35 - 17 in sign-and-magnitude notation.
72. Represent -26 and -17 in 2s-complement notation.
73. Find the value of 35 - 26 and 35 - 17 in 2s-complement notation.
74. Give one reason why 2s-complement notation is the dominant representation for negative numbers in modern computers.

Most instructions in the MIPS processor can be classified as R-format, I-format, and J-format instructions.
75. How many operands does an R-format instruction typically have?
76. Give one example of an R-type format.

77. Give two examples of an I-type format.
78. How many operands does an J-format instruction typically have?
79. Give one example of a J-type format.

Several important components of the datapath are the program counter, instruction memory, the registers, the ALU, and data memory.
80. Why is the ALU essential for many instructions in MIPS?
81. Give one example of an instruction that does not require the ALU.
    Jump instructions are examples of instructions that do not require the use of an adder.
82. Essential to the performance of any computer is the clock. Explain why the clock is an essential component of the datapath.
83. Label the image and give explanations/examples of each:
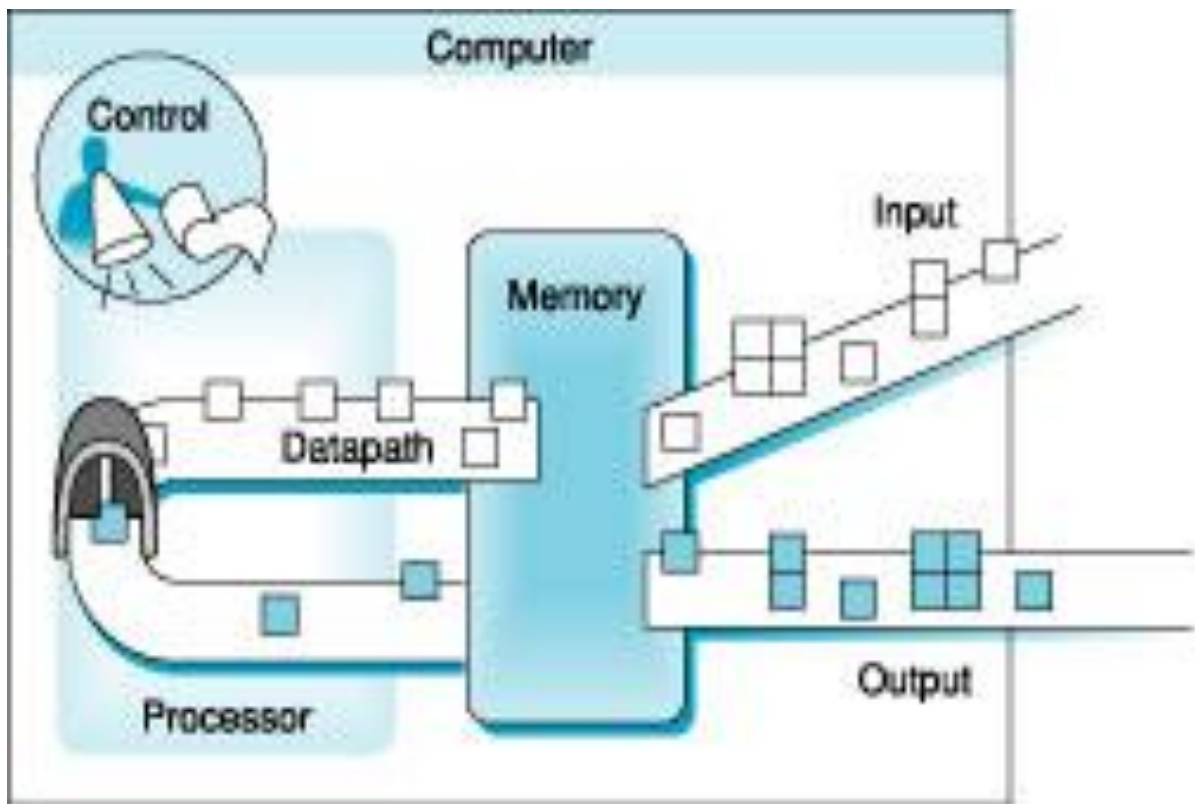

84. Definitions:

    Big Endian:
    Little Endian:
    Power Wall:
   Overflow:
    Underflow:
    ALU:
85. Convert the decimal number 28 into sign and magnitude, 1's complement, 2's complement, octal, and hexidemical.

86. Sign/magnitude, 1's complement, 2's complement for the number -5.
87. Which of the following is an advantage of 2's complement?

- Addition and subtraction are very easy.
- The number can be read directly from the bits that are 1.
- Converting negative numbers to decimal is very easy.
- None of the above

88. Unsigned numbers are convenient for some specific cases (such as counters) because.......
89. What is an advantage of hexadecimal numbers with respect to binary?
90. What are the parts of the instruction cycle?
91. Computer A: Cycle Time = 250ps, CPI = 2.0, Computer B: Cycle Time = 500ps, CPI = 1.2. Which computer can execute each instruction faster?
92. Label the following picture with the major components of a motherboard and related hardware.
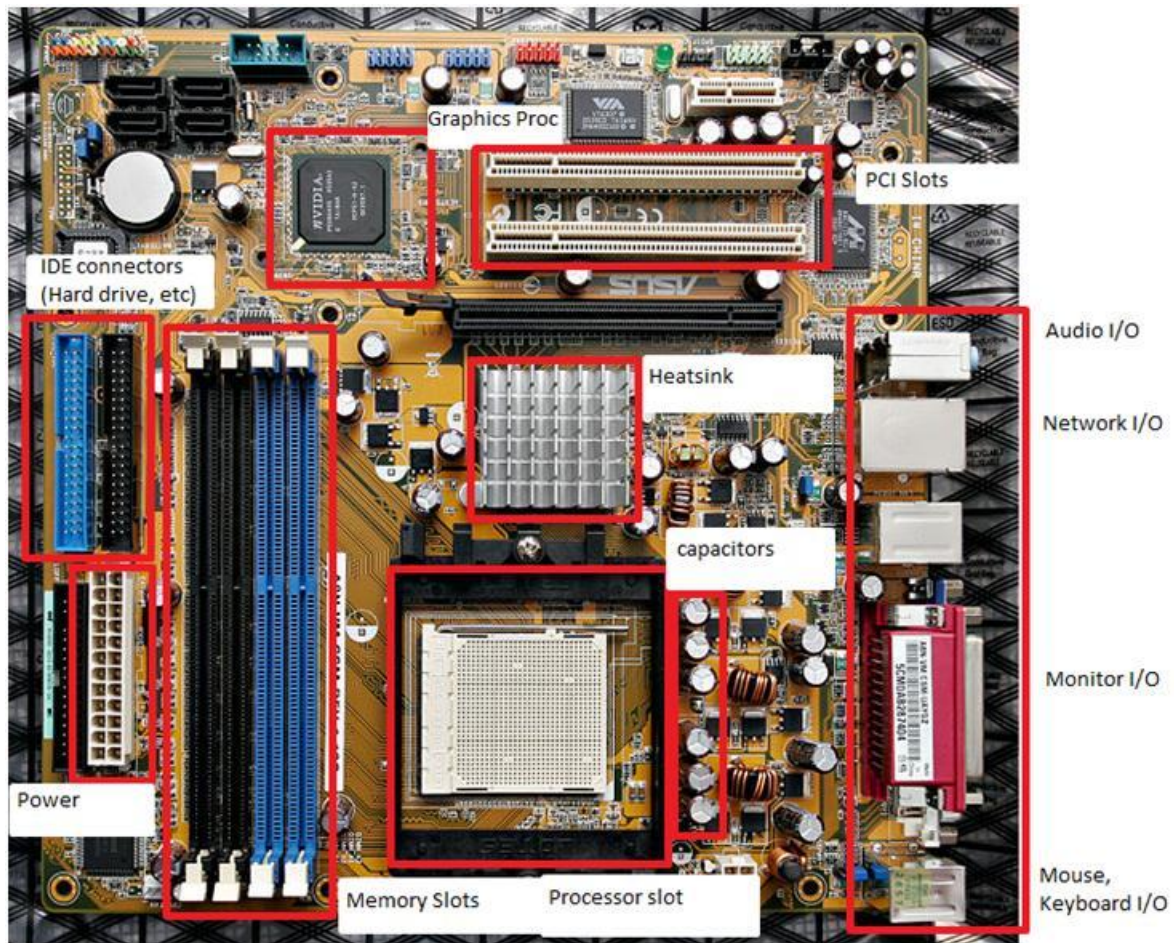
93. Define the following terms: desktop computer, embedded computer, supercomputer.
94. State the differences between embedded and supercomputers by examining only the power equation: (Power) = (Capacitive load [aka: fanout])*(Voltage)2 *(Frequency [aka: clock rate])

95. What are the four underlying principles of hardware design (briefly explain)?

96. Draw a Full Adder using logic gates and write the boolean equations:

97. Write the equation for calculating computer performance (CPU time in seconds):

98. Name several components that affect CPU time performance:

99. Convert this 16-bit hexadecimal number to decimal and binary.

100.   Subtract 1200010 from the above number. Express the result in 2's complement.

101.   What are the labeled parts on this picture?
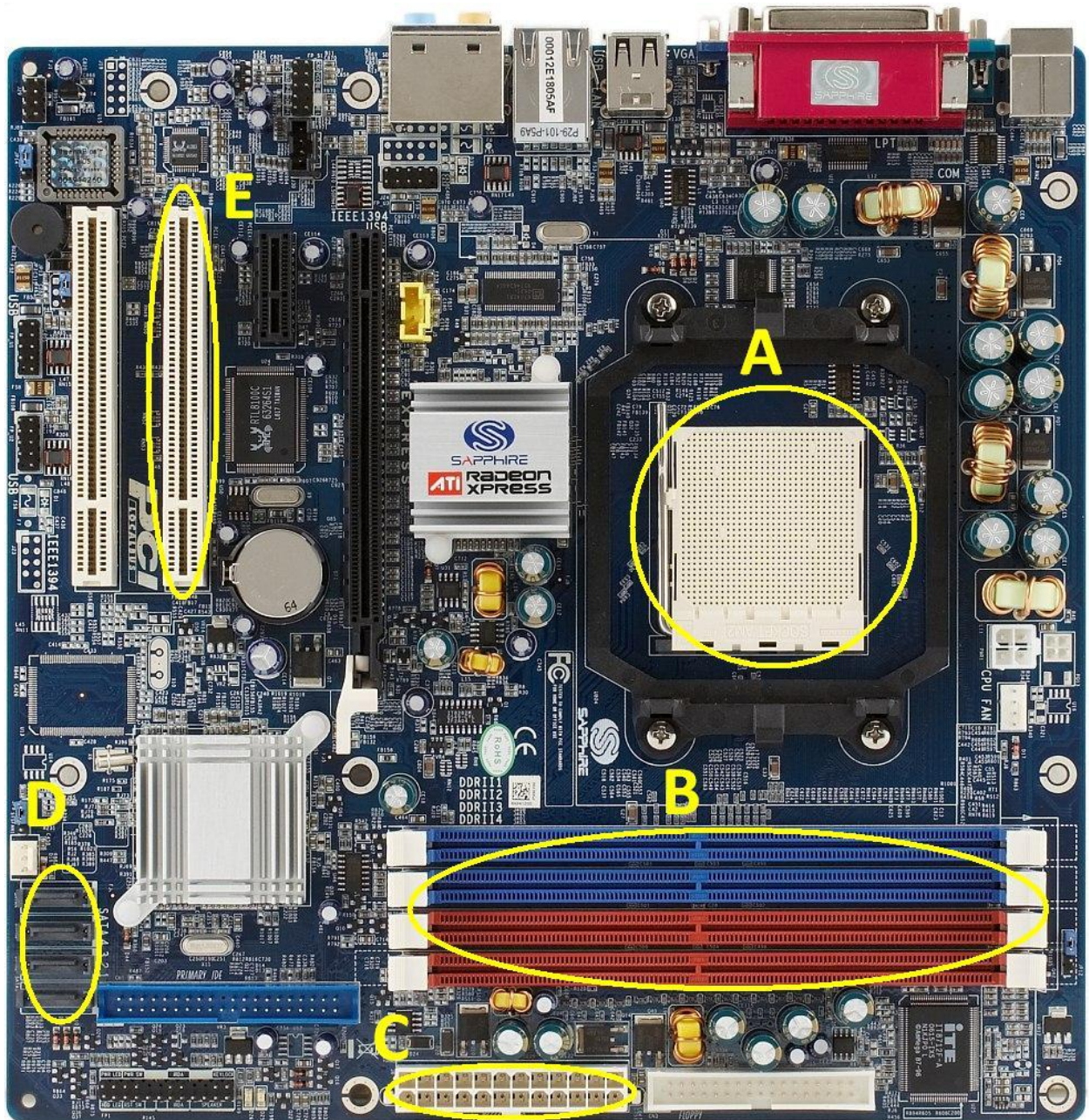
102.   Convert the following numbers into Hexidecimal (Base 16) and then Binary (Base 2):

A) 57
B) 168
C) 40
D) 92

103.   If you convert 178 and 97 into unsigned 8-bit binary numbers and add them together, what do you get?

A) 0b100010011
B) 275
C) 0b10101111
D) 0b00010011
E) An overflow error

104.   What does the following MIPS code do?

add a, b, c
add a, a, d
add a, a, e

105.   What is the largest unsigned integer that can be expressed in: 1 bit?, 1 nybble?, 1 byte?

106.   The following mathematical operation of 2's complement binary in a fixed 8-bit register with no sign extension

             0111 1110
        +   0000 0010

will cause:

- overflow.
- underflow.
- (none of the above)

107.   Identify the line comment that best-describes this MIPS operation


```
SLL $s1, $s2, 3
```

- # shift left logical the contents of $s1 and place into $s2
- # multiply the contents of $s2 by 8 and place into $s1
- # shift left logical the third bit of $s2 and place into $s1
- (none of the above)

108.   2's complement binary

- is difficult to implement in hardware.

- causes an imbalance between the maximum positive number and maximum negative number that can be represented.
- represents its sign in the right-most bit.
- (none of the above)

109. True or False: The ability to represent -0 is a consequence of 2's complement binary.

110. Consider the following MIPS code:

```
FOO:          add $t0, $0, $a0         # the start of the FOO routine
              add $t1, $0, $a1
FOO_a:        beq $t0, $t1, FOO_r      # a loop in the FOO routine
              addi $t0, $t0, 1
              addi $t1, $t1, -1
              b FOO_a
FOO_r:        jr $ra                   # the return of the FOO routine
```

This code
- contains a bug due to improper management of the stack.
- contains a bug due to a syntax error.
- is not useful for any purpose other than "spinning the wheels of the processor".
- returns a value useful to the calling routine.
- (none of the above)

111. What are the basic types of MIPS Assembly instructions?

112. What are the different types of addressing modes does MIPS support?

113. If the number of processors (cores) is doubled in a computer system, the expected output is expected to change:
   A. Twice the original output
   B. Half the original output
   C. Four times the original output
   D. Slightly less than twice the original output

114. Using 2's complement, subtract 0111 from 1001.

115. What hardware components are needed to completed a data path for an "ADD" instruction

116. Explain the power wall problem and how modern computers get around this problem.

117. A program took 20 seconds to complete. During this time, the CPU spent 5 seconds doing load instructions. By how much do the load instructions need to be sped up by to reduce execution time by 20%?

118. Given the following MIPS code:

```
lw $t0, 0($sp)
lw $t1, 4($sp)

bgt $t0, $t1, ExitProgram     Line A
```

```
add, $v0, $t1, $t0
add, $sp, $sp, 8
```

`ExitProgram:` **Line B**

What kind of addressing mode for Line A would the assembler use to jump to Line B, ExitProgram?

119.   The carry look ahead method is able to use parallel execution to speed up adding. What do two consecutive adders share that this method takes advantage of?

120.   Add 1310 and 510 using 1's complement. With a word size of 5 bits, does an overflow occur?

121.   Implement the following Java code in MIPS assembly code:

```
while(a < 10){
    D[a] = b + a;
    a +=1;
}
```

Given:

```
.data

D:    .space 40
inta:     .word 0
intb:     .word 5

.text
.globl main

        #Your Code Here
```

122.   Convert the 12-bit HEX number A17 into 12-bit binary and decimal (assuming unsigned representation).

123.   If this number is represented in 12-bit Sign-and-Magnitude, what decimal number does it represent?

124.   Represent the opposite of the result from part b in 12-bit sign-and-magnitude binary

125.   Represent the result from part b in 12-bit binary one's compliment

126.   Represent the result from part b in 12-bit binary two's compliment

127.   Perform the following actions in MIPS assembly language:
- Place the sum of $t0 and $t1 in $t2
- Increment $t1
- Assuming the address of the base of arrA is in $s1, load arrA[3] element into $t3
- Assuming the address of the base of arrA is in $s1, store $t3 into arrA[12]
- Use the "sll" command to multiply the contents of $s1 by 4 and store it in $t0

128.

Processor	Clock Rate	CPI (Clock Cycles per instruction)
P1	2 GHz	1.0
P2	1.5 GHz	1.5
P3	3 GHZ	2.5

    a. Which processor has the highest performance?
    b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions
    c. What clock rate should each processor have so that if increase the CPI by 20%, the time will be decreased by 30%

129.   Explain what the following MIPS code does:

```
.data
str:    .asciiz "This is a string."
ans:    .asciiz "Length is "
endl:   .asciiz "\n"

.text
.globl main


main:
        la      $t2,str
        li      $t1,0

nextCh: lb      $t0,($t2)
        beq     $t0, $zero strEnd
        add     $t1,$t1,1
        addi    $t2,$t2,1
        j       nextCh

strEnd: la      $a0,ans
        li      $v0,4
        syscall

        move    $a0,$t1
        li      $v0,1
        syscall

        j       $ra
```

130.   By how much is the total time reduced if the time for FP operations is reduced by 20%?

	FP instr	INT instr	L/S instr	Branch Instr	Total Time	REDUCED FP	amount reduced
a	50	100	75	40			
b	80	80	20	40			

131.   If the clock rate is 5GHz and the IPC = .4, what is the MIPS rating?

132.   If A =0E26 and B =B4CA what is their sum if they represent 16 bit unsigned hexadecimal numbers? The result should be in Hexadecimal.
133.   What are A and B in decimal assuming they are a) unsigned? b)sign and magnitude?
134.   What is the sum of A + B when using saturating arithmetic assuming they are 8 bit unsigned numbers?

   A = 11001101
   B = 01011010

135.   Given the information in the following table: Find the clock rate for P2 that reduces its execution time to that of P2.

Processor	Clock Rate	No. Instructions	Time
P1	2 GHz	40×10^9	8 s
P2	1.5 GHz	50×10^9	9 s

136.   What is the corresponding MIPS assembly code for the C statement: $f = g - (f + h)$
137.   What is the corresponding MIPS assembly code for the C loop below:

            while (save [i] == x)
   i+=1;

138.   Add the following 8 bit numbers in unsigned, signed and two's complement and state whether there is an overflow underflow or neither.

        15 and 7 unsigned
        -15 and 7 signed and twos complement

139.   List some pros and cons of incorporating more registers in a computer architecture, and would it be feasible to eliminate main memory (RAM) and use more registers and cache?
140.   Explain the ripple carry adder and when it may be appropriate to use and when it is not appropriate to use?
141.   List and explain the four design principals.
142.   Pertaining to the Power Wall, where: $Power = Capacitive\ Load * voltage^2 * Frequency\ Switched$. Why is it not possible to decrease voltage, as it has been done in the past? What else has been done to address the Power Wall?
143.   In response to the Power Wall, CPU clock rates have not risen but fallen, yet computer performance has not, explain this phenomenon?

144. Connect the following hardware components to form the data path for a simple add instruction. Make sure that your data path correctly performs the fetch, increment, decode, and execution portions of the instruction cycle.
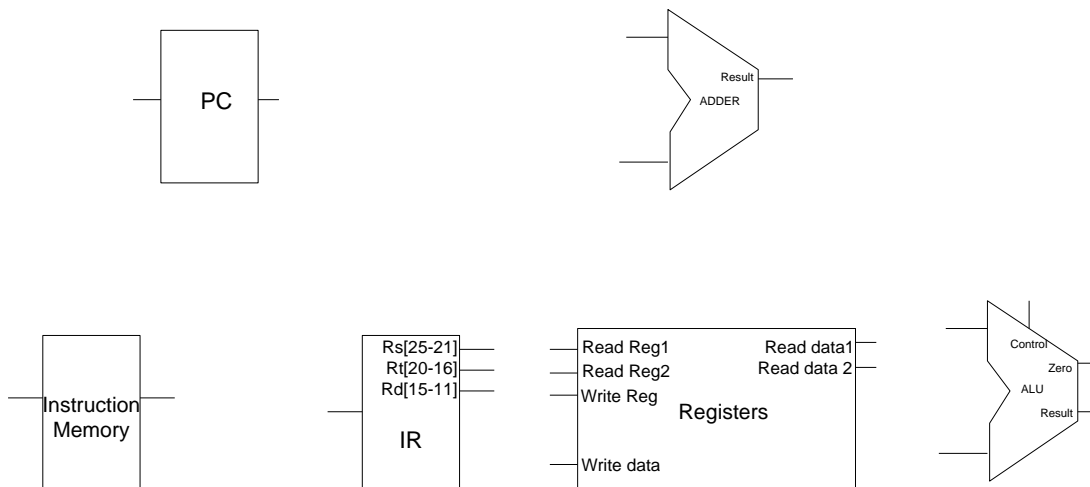
145. Convert the following C (or Java) snippet into MIPS. Assume that the variable i is a temporary variables and can be stored in register t0, j is an additional temporary variable which can be stored in register t1.

```
int i = 0;
int j = 0;
for( i = 0; i < 100; i++)
{
        j += i;
}
```

146. Which of the following instructions would have a type I instruction format?
   - add $t0 $t1 $t2
   - jal end_loop
   - sw $t0, 0($t1)
   - jr $ra

147. Of the following list of registers, circle all the registers that must be preserved by the callee MIPS function?
   - $t0 - $t9
   - $s0 - $s7
   - $a0 - $a3
   - $v0 - $v1
   - $sp
   - $ra

148. Convert the following binary number into hexadecimal (be sure to include the correct subscript).

$$1111 \quad 1001 \quad 1010 \quad 0000 \quad 0100 \quad 0010 \quad 1011 \quad 1101_2$$

149.   What are the five classic computer components?

150.   Convert each decimal number to 8-bit 2's complement:

- 30
- -100
- 87
- -33
- -46

151.   Circle or highlight each arithmetic instruction that causes an exception on overflow:

   add   addu   addi   addiu   sub   subu

152.   Write MIPS code to add two unsigned integers from registers $s0 and $s1 together, multiply the result (in an unsigned way) by the value in register $s2, and store that result into both register $s4 and the memory location referenced in $s3. For this problem, assume that callee-saved registers have already been saved (and later restored) for you.

153.   Draw a truth table for the following logic equation and simplify the equation (suggestion: use either simplification methods or a Karnaugh Map): Z = (A AND B) OR (A OR (B AND C)). Written using symbols: Z = AB + (A + BC)

Two processors take the following number of clock cycles for each instruction. Each processor's maximum clock speed and power consumption are also shown.

Processor	arithmetic	load	store	branch	floating point	clock speed	power consumption
P1	1	2	2	2	10	1.0 GHz	9W
P2	2	6	6	3	2	4.0 GHz	35W
P3	1	4	4	2	1	1.5 GHz	15W

154.   For code that executes an equal number of arithmetic, load, store, branch, and floating point operations, calculate each processor's average number of instructions per second. In that respect, which processor is fastest?

155.   For the same code, calculate the amount of energy consumed for each instruction. In that respect, which processor has the least energy consumption?

156.   Express the following 8-bit numbers using one's complement and two's complement notations, and then add them together: 100 and -5. Express the final answer in decimal and state whether an overflow has occurred.

157.   Express the following 8-bit numbers using one's complement and two's complement notations, and then add them together: -57 and -71. Express the final answer in decimal and state whether an overflow has occurred.

Consider two computers that each run 2 x 109 instructions:
- Computer A has a clock rate of 2 GHz and a CPI of 2.5
- Computer B has a clock rate of 2.5 GHz and a CPI of 3.0

158.   Which computer is faster and by how much? What must the CPI of the slower computer be reduced to in order to match the execution time of the faster computer?

Consider the following specifications of a program:
- There are 5×10^6 instructions of Type A and the CPI is 2.0
- There are 6×10^6 instructions of Type B and the CPI is 2.5
- There are 7×10^6 instructions of Type C and the CPI is 3.0

159. If the clock rate of the computer is 2 GHz, determine the CPU execution time of the program.

160. Convert the following C code to MIPS:

array[2] = array[1] - i + 5;
The base address of array is in $s0 and variable i is in $s1.